What is claimed is:

1. A method for creating a gettering site in a semiconductor wafer, comprising:

forming a predetermined arrangement of a plurality of holes in the semiconductor wafer through a surface of the wafer; and

annealing the wafer such that the wafer undergoes a surface transformation to transform the arrangement of the plurality of holes into a predetermined arrangement of at least one empty space within the wafer, the at least one empty space having a predetermined size, wherein the at least one empty space forms the gettering site.

2. The method of claim 1, wherein forming a predetermined arrangement of a plurality of holes includes forming a predetermined arrangement of a plurality of cylindrical holes, each cylindrical hole having a predetermined length and diameter to form the at least one empty space upon annealing.

3. The method of claim 2, wherein forming a predetermined arrangement of a plurality of cylindrical holes includes forming the plurality of cylindrical holes with a length that is approximately equal to an integer of a critical length (λ_C), the critical length being dependent on a radius (R_C) of the cylindrical hole.

4. The method of claim 2, wherein the at least one empty space includes a sphere-shaped void.

5. The method of claim 2, wherein the at least one empty space includes a pipe-shaped void.

6. The method of claim 2, wherein the at least one empty space includes a plate-shaped void.

7. The method of claim 1, wherein the at least one empty space includes a plurality of voids that form a gettering region in a crystalline semiconductor volume of the wafer, each void having an interior surface with dangling bonds, the plurality of voids having a shape and an arrangement predetermined to have a large ratio between the interior surface and the volume.

8. The method of claim 1, wherein the semiconductor wafer includes a bulk semiconductor wafer.

9. The method of claim 1, wherein the semiconductor wafer includes a semiconductor-on-insulator (SOI) wafer.

10. A method for creating a proximity gettering site in a silicon wafer, comprising:

forming a predetermined arrangement of a plurality of holes in the silicon wafer through a surface of the wafer; and

annealing the wafer such that the wafer undergoes a surface transformation to transform the arrangement of the plurality of holes into a predetermined arrangement of at least one void within a volume of the wafer, the at least one void having a predetermined size and an interior surface with dangling bonds, wherein the at least one void forms the gettering site and the at least one void has a predetermined shape and arrangement to have a large ratio between the interior surface and the volume.

11. The method of claim 10, wherein forming a predetermined arrangement of a plurality of holes includes forming a predetermined arrangement of a plurality of cylindrical holes, each cylindrical hole having a predetermined length and diameter to form the at least one empty space upon annealing.

12. The method of claim 11, wherein forming a predetermined arrangement of a plurality of cylindrical holes includes forming the plurality of cylindrical holes with a length that is approximately equal to an integer of a critical length (λ_C), the critical length being dependent on a radius (R_C) of the cylindrical hole.

13. The method of claim 10, wherein the at least one void includes a sphere-shaped void.

14. The method of claim 10, wherein the at least one void includes a pipe-shaped void.

15. The method of claim 10, wherein the at least one void includes a plate-shaped void.

16. The method of claim 10, wherein the silicon wafer includes a bulk silicon wafer.

17. The method of claim 10, wherein the silicon wafer includes a silicon-on-insulator (SOI) wafer.

18. A method for forming a semiconductor structure, comprising:

precisely forming a plurality of holes through a surface of a semiconductor substrate in a precise arrangement;

annealing the semiconductor substrate such that the plurality of holes are transformed into at least one predetermined void in a gettering region within the semiconductor substrate; and

performing semiconductor fabrication processes to form a semiconductor device in a device region proximate to the gettering region,

wherein defects generated by the at least one void getters unwanted impurities from the device region during the semiconductor fabrication processes.

19. The method of claim 18, wherein precisely forming a plurality of holes through a surface of a semiconductor substrate in a precise arrangement includes forming the plurality of holes such that, upon annealing, the plurality of holes are transformed to form a plurality of sphere-shaped voids in the gettering region.

20. The method of claim 18, wherein precisely forming a plurality of holes through a surface of a semiconductor substrate in a precise arrangement includes forming the plurality of holes such that, upon annealing, the plurality of holes are transformed to form at least one pipe-shaped void in the gettering region.

21. The method of claim 18, wherein precisely forming a plurality of holes through a surface of a semiconductor substrate in a precise arrangement includes forming the plurality of holes such that, upon annealing, the plurality of holes are transformed to form at least one plate-shaped void in the gettering region.

22. The method of claim 18, wherein precisely forming a plurality of holes includes precisely forming a plurality of cylindrical holes, each cylindrical hole having a predetermined length and diameter to form the at least one predetermined void upon annealing.

23. The method of claim 18, wherein precisely forming a plurality of holes includes forming each of the holes with a length that is approximately equal to an integer of a critical length (λ_C) dependent on a hole radius (R_C).

24. The method of claim 18, wherein:

precisely forming a plurality of holes includes forming each of the holes with a length that is not approximately equal to an integer of a critical length (λ_C) dependent on a hole radius (R_C), and

performing semiconductor fabrication processes includes polishing a top surface of the semiconductor substrate in preparation to form the semiconductor device.

25. The method of claim 24, wherein performing semiconductor fabrication processes further includes depositing a crystalline silicon layer after polishing the top surface of the semiconductor substrate.

26. A method for forming a silicon structure, comprising:

precisely forming a plurality of holes through a surface of a silicon substrate in a precise arrangement;

annealing the crystalline semiconductor such that the plurality of holes are transformed into at least one predetermined void in a gettering region within the semiconductor; and

performing semiconductor fabrication processes to form a semiconductor device in a device region proximate to the gettering region,

wherein defects generated by the at least one void getters unwanted impurities from the device region during the subsequent semiconductor fabrication processes.

27. The method of claim 26, wherein precisely forming a plurality of holes through a surface of a semiconductor substrate in a precise arrangement includes forming the plurality of holes such that, upon annealing, the plurality of holes are transformed to form a plurality of sphere-shaped voids in the gettering region.

28. The method of claim 26, wherein precisely forming a plurality of holes through a surface of a semiconductor substrate in a precise arrangement includes forming the plurality of holes such that, upon annealing, the plurality of holes are transformed to form at least one pipe-shaped void in the gettering region.

29. The method of claim 26, wherein precisely forming a plurality of holes through a surface of a semiconductor substrate in a precise arrangement includes forming the plurality of holes such that, upon annealing, the plurality of holes are transformed to form at least one plate-shaped void in the gettering region.

30. The method of claim 26, wherein precisely forming a plurality of holes includes precisely forming a plurality of cylindrical holes, each cylindrical hole having a predetermined length and diameter to form the at least one predetermined void upon annealing.

31. The method of claim 26, wherein precisely forming a plurality of holes includes forming each of the holes with a length that is approximately equal to an integer of a critical length (λ_C) dependent on a hole radius (R_C).

32. The method of claim 26, wherein:

precisely forming a plurality of holes includes forming each of the holes with a length that is not approximately equal to an integer of a critical length (λ_C) dependent on a hole radius (R_C), and

performing semiconductor fabrication processes includes polishing a top surface of the semiconductor substrate in preparation to form the semiconductor device.

33. The method of claim 32, wherein performing semiconductor fabrication processes further includes depositing a crystalline silicon layer after polishing the top surface of the semiconductor substrate.

34. A method for preparing a wafer for semiconductor device fabrication:

forming a predetermined arrangement of a plurality of holes in the semiconductor wafer through a surface of the wafer; and

annealing the wafer such that the plurality of holes are transformed into a predetermined arrangement of at least one void within a predetermined gettering volume in the wafer, the at least one void having a predetermined size and shape with an interior surface area, the predetermined arrangement, size and shape being selected to provide a large interior surface area to gettering volume ratio to enhance gettering of a device region in the wafer.

35. The method of claim 34, further comprising forming a crystalline semiconductor layer on the wafer such that at least a portion of the crystalline semiconductor layer over the gettering volume functions as the device region.

36. The method of claim 34, wherein forming the predetermined arrangement of a plurality of holes includes forming a plurality of holes with a predetermined size and shape and at a predetermined location such that, upon annealing, the at least one void in the predetermined gettering volume is proximate to the device region.

37. The method of claim 34, wherein the predetermined gettering volume entirely spans across a majority of a wafer area.

38. The method of claim 34, wherein the predetermined gettering volume includes a plurality of gettering volumes and the device region includes a plurality of device regions, each gettering volume being proximately located to at least one device region.

39. A method for forming a transistor, comprising:

forming a proximity gettering region to be proximate to a crystalline semiconductor region in a wafer, the proximity gettering region including a precise arrangement of precisely-formed voids to getter impurities from the crystalline semiconductor region;

forming a gate dielectric over the crystalline semiconductor region;

forming a gate over the gate dielectric; and

forming a first diffusion region and a second diffusion region in the crystalline semiconductor region, the first and second diffusion regions being separated by a channel region formed in the crystalline semiconductor region between the gate and the proximity gettering region.

40. The method of claim 39, wherein forming a proximity gettering region to be proximate to a crystalline semiconductor region in a wafer includes:

forming a predetermined arrangement of a plurality of holes in the wafer through a surface of the wafer; and

annealing the wafer to transform the predetermined arrangement of the plurality of holes into a predetermined arrangement of at least one void of a predetermined size and shape to form the proximity gettering region in the wafer.

41. The method of claim 39, wherein the precisely-formed voids includes a sphere-shaped void.

42. The method of claim 39, wherein the precisely-formed voids includes a pipe-shaped void.

43. The method of claim 39, wherein the precisely-formed voids includes a plate-shaped void.

44. The method of claim 39, wherein the crystalline semiconductor region includes a crystalline silicon region.

45. A method for forming a memory device, comprising:

forming a gettering region in a semiconductor substrate, the gettering region including a precise arrangement of precisely-formed voids to getter impurities from a crystalline semiconductor region of the substrate;

forming a memory array in the crystalline semiconductor region, including forming a plurality of memory cells in rows and column and forming at least one transistor for each of the plurality of memory cells;

forming a plurality of word lines, including connecting each word line to a row of memory cells;

forming a plurality of bit lines, including connecting each bit line to a column of memory cells; and

forming control circuitry, including forming word line select circuitry and bit line select circuitry for use to select a number of memory cells for writing and reading operations.

46. The method of claim 45, wherein at least one of forming the memory array and forming the control circuitry includes forming at least one transistor using the crystalline semiconductor region, including:

forming a gate dielectric over the crystalline semiconductor region;

forming a gate over the gate dielectric; and

forming a first diffusion region and a second diffusion region in the crystalline semiconductor region, the first and second diffusion regions being separated by a channel region formed in the crystalline semiconductor region between the gate and the gettering region.

47. The method of claim 45, wherein forming a gettering region in a semiconductor substrate includes:

forming a predetermined arrangement of a plurality of holes in the semiconductor wafer through a surface of the wafer; and

annealing the wafer such that the plurality of holes are transformed into a predetermined arrangement of at least one void within a volume of the gettering region, the at least one void having a predetermined size and shape with an interior surface area, the predetermined arrangement, size and shape being selected to provide a large interior surface area to volume ratio to enhance gettering of the crystalline semiconductor region.

48. A semiconductor wafer, comprising:

at least one device region; and

at least one gettering region located proximate to the at least one device region, the at least one gettering region including a precisely-determined arrangement of a plurality of precisely-formed voids formed within the wafer using a surface transformation process.

49. The wafer of claim 48, wherein the at least one gettering region includes one gettering region to getter the entire wafer.

50. The wafer of claim 48, wherein the at least one gettering region includes a plurality of gettering regions positioned under a plurality of device regions.

51. The wafer of claim 48, wherein the precisely-determined arrangement of a plurality of voids is uniformly distributed through the at least one gettering region.

52. The wafer of claim 48, wherein the plurality of voids are separated by a critical length (λ_C) that is dependent on a radius (R_C) of a number of holes used to form the plurality of voids using a surface transformation process.

53. The wafer of claim 48, wherein each of the voids has an interior surface that includes dangling bonds such that the plurality of voids getter impurities from the at least one device region.

54. The wafer of claim 53, wherein:

the at least one gettering region has a volume; and

the precisely-determined arrangement of the plurality of precisely-formed voids is formed to provide a large ratio between the interior surface of the plurality of precisely-formed voids and the volume to enhance gettering.

55. The wafer of claim 48, wherein the plurality of precisely-formed voids includes a sphere-shaped void.

56. The wafer of claim 48, wherein the plurality of precisely-formed voids includes a pipe-shaped void.

57. The wafer of claim 48, wherein the plurality of precisely-formed voids includes a plate-shaped void.

58. The wafer of claim 48, wherein the at least one device region includes a plurality of device regions and the at least one gettering region includes a plurality of gettering regions.

59. The wafer of claim 48, wherein the at least one device region extends across a majority of a wafer area.

60. A semiconductor structure, comprising:

a gettering region proximate to a device region in a semiconductor wafer;

the gettering region including a precisely-determined arrangement of a plurality of precisely-formed voids through a surface transformation process, each of the voids having an interior surface that includes dangling bonds such that the plurality of voids getter impurities from the at least one device region;

a transistor formed using the device region, the transistor including

a gate dielectric over the device region;

a gate over the gate dielectric; and

a first diffusion region and a second diffusion region formed in the device region, the first and second diffusion regions being separated by a channel region formed in the device region between the gate and the proximity gettering region.

61. The structure of claim 60, wherein the plurality of voids are separated by a critical length (λ_C) that is dependent on the radius (R_C) of a number of holes used to form the plurality of voids using the surface transformation process.

62. The structure of claim 60, wherein the precisely-determined arrangement of a plurality of voids is uniformly distributed through the at least one gettering region.

63. The wafer of claim 60, wherein the plurality of precisely-formed voids includes a sphere-shaped void.

64. The wafer of claim 60, wherein the plurality of precisely-formed voids includes a pipe-shaped void.

65. The wafer of claim 60, wherein the plurality of precisely-formed voids includes a plate-shaped void.

66. A memory device, comprising:

at least one gettering region formed in a semiconductor substrate, the gettering region including a precise arrangement of precisely-formed voids to getter impurities from a crystalline semiconductor region of the substrate;

a memory array formed in the crystalline semiconductor region, including a plurality of memory cells formed in rows and columns, and at least one transistor for each of the plurality of memory cells;

a plurality of word lines, each word line being connected to a row of memory cells;

a plurality of bit lines, each bit line being connected to a column of memory cells; and

control circuitry, including word line select circuitry and bit line select circuitry to select a number of memory cells for writing and reading operations.

67. The device of claim 66, wherein the precise arrangement of the plurality of voids is uniformly distributed through the gettering region.

68. The device of claim 66, wherein the plurality of voids are separated by a critical length (λ_C) that is dependent on a radius (R_C) of a number of holes used to form the plurality of voids using a surface transformation process.

69. The device of claim 66, wherein each of the voids has an interior surface that includes dangling bonds such that the plurality of voids getter impurities from the at least one device region.

70. The device of claim 69, wherein:

the gettering region has a volume; and

the precisely-determined arrangement of the plurality of precisely-formed voids is formed to provide a large ratio between the interior surface of the plurality of precisely-formed voids and the volume to enhance gettering of the crystalline semiconductor region.

71. The wafer of claim 66, wherein the plurality of precisely-formed voids includes a sphere-shaped void.

72. The wafer of claim 66, wherein the plurality of precisely-formed voids includes a pipe-shaped void.

73. The wafer of claim 66, wherein the plurality of precisely-formed voids includes a plate-shaped void.